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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,381	07/09/2003	Douglas Brisbin	NSC1-M2900 [P05632]	1278

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EXAMINER

LANDAU, MATTHEW C

ART UNIT PAPER NUMBER

2815

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/616,381

Applicant(s)

BRISBIN ET AL.

Examiner

Matthew Landau

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 November 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 10/27/2003.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION***Drawings***

Figure 4a should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 4 and 12 objected to because of the following informalities: the limitation "the source region face depth and the source region face depth" should be changed to "the source region face depth and the drain [[source]] region face depth". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, 5, 8, 9, 12, and 13 are rejected under 35 U.S.C. 102(a) as being anticipated by Strachan et al. (US Pat. 6,566,710, hereinafter Strachan).

In regards to claim 1, Figures 7 and 10A of Strachan disclose an LDMOS transistor array structure comprising: an array that includes a plurality of alternating source regions 632 and a plurality of alternating drain regions 620 formed in a semiconductor substrate to define a checkerboard pattern of said alternating source and drain regions, wherein at least a first source region (middle source region) of the alternating source regions includes a first source region face (bottom side of hexagon) which is orientated toward a first drain region face (top side) of a first drain region (drain region in bottom row) of the plurality of alternating drain regions, and wherein the first drain region face has a drain region face length and the source region face has a source region face length, and wherein the drain region face length is greater than the source region face length (the top side of the drain region is slightly longer than the bottom side of the hexagonal source region); a conductive source region interconnect 652 structure formed in electrical contact with each of the plurality of alternating source regions in the array to electrically connect said source regions in parallel; and a conductive drain region interconnect structure 650 formed in electrical contact with each of the plurality of alternating drain regions in the array to electrically connect said drain regions in parallel (col. 4, lines 49-53).

In regard to claims 4, 8, and 12, Figure 7 of Strachan discloses the source region 632 face has a source region face depth, and the drain region 620 face has a face depth, and the source region face depth and the drain region face depth are substantially equal in length. Figure 7 disclose the source and drain regions have the same depth. Therefore, the respective face depths must be equal.

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In regards to claims 5 and 13, Figure 10A of Strachan discloses each of the alternating source regions has four source region faces, and each of the source region faces has the same source region face length, and wherein each of the alternating drain regions has four faces, and each of the drain region faces has the same drain region face length.

In regards to claim 9, Figures 7 and 10A of Strachan disclose a high power transistor including: a source region 632 (middle region) which includes a first source region face (bottom side of hexagon) wherein the source region face has a source region face length; a drain region (region in bottom row) 620 which includes a first drain region face (top side) wherein the drain region face has a drain region face length; a source contact 652 coupled with the source region; a drain contact 650 coupled with the drain region; a channel region disposed between the source region and the drain region; a channel region disposed between the source region and the drain region; wherein in response to a voltage applied across the source contact and the drain contact electrons flow from the source region to the drain region; and wherein the drain region face length is longer than the source region face length (the top side of the drain region is slightly longer than the bottom side of the hexagonal source region).

Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Hoshi et al. (US Pat. 5,635,742, hereinafter Hoshi).

In regards to claims 1-3, 6, and 7, Figures 2 and 3A of Hoshi disclose an LDMOS transistor array structure comprising: an array that includes a plurality of alternating source regions (6 or S) and a plurality of alternating drain regions (8 or D) formed in a semiconductor substrate 1 to define a checkerboard pattern of said alternating source and drain regions, wherein

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at least a first source region of the alternating source regions includes a first source region face (side) which is orientated toward a first drain region face (side) of a first drain region of the plurality of alternating drain regions, and wherein the first drain region face has a drain region face length and the source region face has a source region face length, and wherein the drain region face length is at least twice as long as the source region face length; a conductive source region interconnect 12 structure formed in electrical contact with each of the plurality of alternating source regions in the array to electrically connect said source regions in parallel; and a conductive drain region interconnect structure 15 formed in electrical contact with each of the plurality of alternating drain regions in the array to electrically connect said drain regions in parallel. As shown in Figure 3A, the source regions come in groups of four. For the purposes of this Office Action, it is considered only the lower left source region in each group is part of the “plurality of alternating source regions”. Thus, the drain regions and each of these source regions form a checkerboard pattern. It is clear from Figure 3A that each side of the drain regions is at least twice as long as each side of the aforementioned source regions.

In regards to claims 4, 8, and 12, Figure 2 of Hoshi discloses the source region 6 face has a source region face depth, and the drain region 8 face has a face depth, and the source region face depth and the drain region face depth are substantially equal in length.

In regards to claims 5 and 13, Figure 3A of Hoshi discloses each of the alternating source regions S has four source region faces, and each of the source region faces has the same source region face length, and wherein each of the alternating drain regions D has four faces, and each of the drain region faces has the same drain region face length.

In regards to claims 9-11, Figures 2 and 3A of Hoshi disclose a high power transistor including: a source region (6 or S) which includes a first source region face wherein the source region face has a source region face length; a drain region (8 or D) which includes a first drain region face wherein the drain region face has a drain region face length; a source contact S coupled with the source region; a drain contact D coupled with the drain region; a channel region disposed between the source region and the drain region; a channel region disposed between the source region and the drain region; wherein in response to a voltage applied across the source contact and the drain contact electrons flow from the source region to the drain region; and wherein the drain region face length is longer than the source region face length. It is clear from Figure 3A that the length of drain region face is at least twice as long as the source region face.

Claims 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishibe et al. (US PGPub 2002/0072159, hereinafter Nishibe).

In regards to claims 9, 10, and 11, Figure 9 of Nishibe discloses a high power transistor including: a source region 54 which includes a first source region face wherein the source region face has a source region face length; a drain region 55 which includes a first drain region face wherein the drain region face has a drain region face length; a source contact S coupled with the source region; a drain contact D coupled with the drain region; a channel region disposed between the source region and the drain region; a channel region disposed between the source region and the drain region; wherein in response to a voltage applied across the source contact and the drain contact electrons flow from the source region to the drain region; and wherein the drain region face length is longer than the source region face length. Note that although Figure 9

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is merely a cross-section of the device, it can be considered that the cross-sectional area of the source and drain regions shown by the figure are the respective face regions. It is clear from Figure 9 that the length of drain region face is at least twice as long as the source region face.

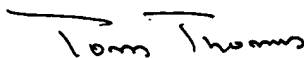
In regards to claim 12, Figure 9 of Nishibe discloses the source region 632 face has a source region face depth, and the drain region 620 face has a face depth, and the source region face depth and the drain region face depth are substantially equal in length.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.


TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Matthew C. Landau
Examiner

September 15, 2004